# SYSTEMS FOR SELECTIVELY DISABLING TIMING VIOLATIONS IN HARDWARE DESCRIPTION LANGUAGE MODELS OF INTEGRATED CIRCUITS AND METHODS OF OPERATING THE SAME

## SUBSTITUTE ABSTRACT

# SYSTEMS FOR SELECTIVELY DISABLING TIMING VIOLATIONS IN HARDWARE DESCRIPTION LANGUAGE MODELS OF INTEGRATED CIRCUITS AND METHODS OF OPERATING THE SAME

## ABSTRACT OF THE DISCLOSURE

There is disclosed an IC simulation system operable to (i) store a plurality of HDL modules, each of which is representative of a circuit element, (ii) receive a HDL description of a desired circuit, and (iii) synthesize a circuit netlist as a function of the received HDL circuit description and ones of the plurality of HDL modules, the circuit netlist is responsible for defining behavioral relationships among associated ones of the HDL modules, and associate a timing-violation controller with the circuit netlist to ignore selected timing violations sensed as a function of various ones of the behavioral relationships during simulation of the desired circuit.